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Crosstalk Analysis of On-chip VLSI Interconnects

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Abstract: In this paper dynamic crosstalk is analyzed for coupled on-chip VLSI interconnects in different conditions. The proposed work has taken the MOS transistor analytical expressions. In this work, calculated the transition delays and different timings of the interconnect aggressor and interconnect victim drivers for in-phase switching and out-of-phase switching. All the calculated results are compared with simulations in SPICE. The average error in the transmission delay using SPICE is 2.02 and 3.274% for the interconnect aggressor and interconnect victim buffers for in phase switching, respectively. The average errors in the same are 2.3 and 1.87% for out phase switching event.

Keywords: CMOS inverter, Crosstalk, Interconnect, Power dissipation

1 INTRODUCTION

As VLSI advancements into sub-micron interconnect wire will play an important role in the overall delay performance and analysis of power consumption of better chips. Interconnect transmission delay will have more impact device delay and make a performance bottleneck [1-5]. For a greater number of interconnect wires and their amount of resistance and resources may require lot to drive the wires may also increases. Hence, increasing the amount of power dissipation integrated circuits. As improvement in technology or scaling will leads to have also provides in a significant may increase in parasitic in interconnects wires [6-12]. Inductive effect and capacitive coupling effect gives interconnect wire coupling crosstalk significant and cause many signal integrity problems. Hence, interconnect wire down scaling is thus careful to be the real contest to CMOS scaling [12-19].

Low power requirement is prominent for todays all electronics equipment and it hold many challenges and design issues [20-22]. To avoid crosstalk noise and decrease the transition delays is major challenge in scaled device as technology nodes decreases. The proposed methods approach gives high accuracy and analytical numerical things used in simulators. The proposed method also provides physical device parameters which are upsetting the transient behaviour. Further, the proposed analytical method can also be applied to multiple logic gates using CMOS logic, later clocking block networks are based on CMOS inverter. The proposed method establishes that the simulation results of the current analysis may be highly good in developing low power design circuits.

2 DESIGNING OF INTERCONNECT WITH DRIVER AND LOAD

For analyzing transition delays of interconnect wires at different switching events, here designed the interconnects with CMOS drivers. CMOS inverters are used as driver and load in this analysis. Equivalent parasitic are used for designing the interconnect. Equivalent RLC parameters are calculated from the mathematical expressions. Here considered the two switching events, they are in-phase switching and out-phase switching. Fig. 1 represents the in-phase switching. In in-phase switching, the input signal triggers in the same level (logic 0 or logic1) at both drivers. During in-phase switching, the effect of crosstalk and delay is very less compared to out-phase switching which has shown in the result analysis. Fig. 2 represents the Out-phase switching of coupled interconnects. During out-phase switching event, the input signals triggers with different logic levels. Hence the delay and crosstalk are more compared to in-phase switching due to the more coupling capacitance induced in the interconnect.

3 RESULT ANALYSIS

In this work, proposed methods are validated using SPICE simulations. For CMOS inverter, the width of the PMOS channel has taken the 2.5 times that of width of NMOS because the mobility difference. The values of parasitic capacitances and resistances values are extracted from the mathematical expressions for different interconnect lines. The extracted interconnect parasitic are $R1 = R2$ =208.93ohms (resistances) and (capacitances) C1=C2 =301.475 fF, Cc (coupling capacitance) of 105.4 fF. For ramp, Wp2 of 0.4µm and slow ramp, Wp2= 10µm has considered. All the results are matched with the simulations. All these parasitic values are generated from the MATLAB and simulation setup has made based on these values. The driver, interconnect and load system has designed based these calculated values. From this, concluded that out-phase switching offering more coupling capacitance due to the triggering of the different signal levels at input side.

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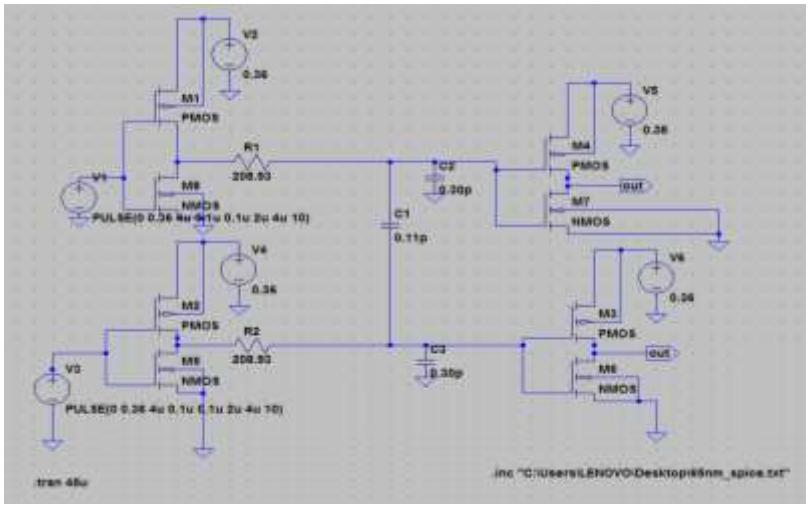

Fig. 1. Circuit diagram of in-phase switching

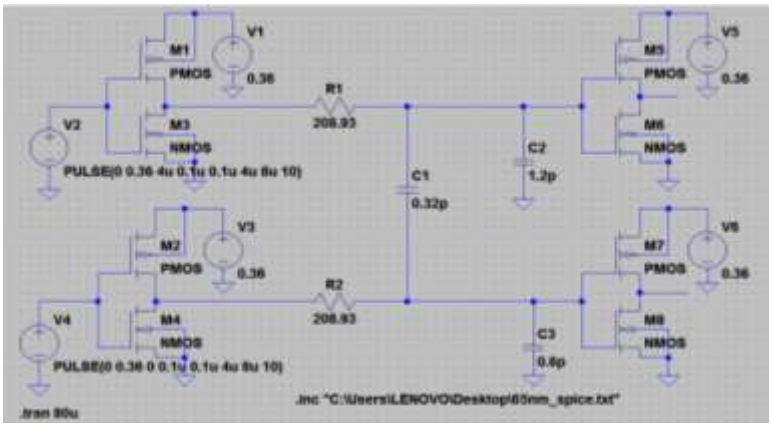

Fig. 2. Circuit diagram of out-phase switching

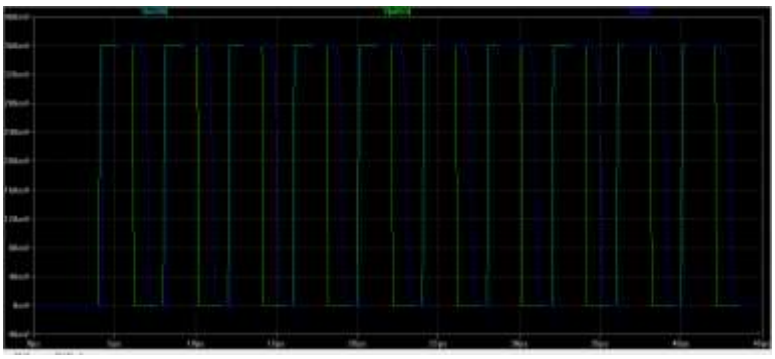

Fig. 3. Output of aggressor line for in-phase switching

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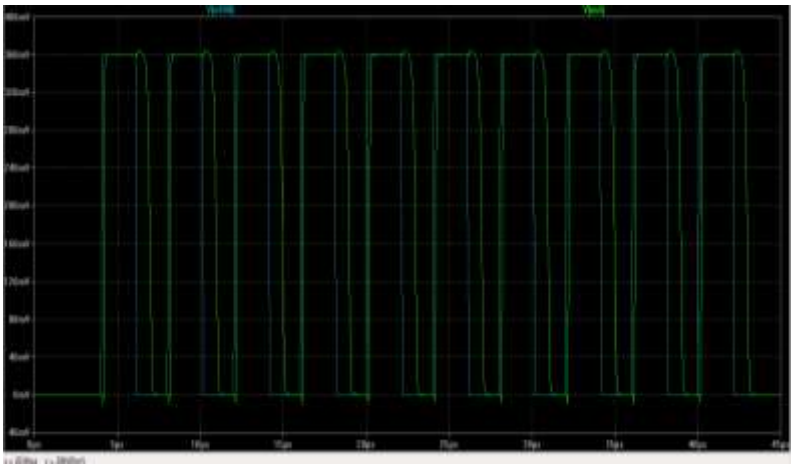

Fig. 4. Output of victim line for in-phase switching

For in-phase analysis, both the inputs given for aggressor interconnect line and victim interconnect line are equal i.e., both are switched from zero to one. Since the circuit represents a buffer, the output should be same as input. Some propagation delay is obtained due of the presence of interconnect coupling capacitance. For out of phase analysis, the inputs given for aggressor interconnects line and victim interconnect line are not same. Aggressor is switched from zero to one and victim is switched from one to zero. The outputs should be same as their respective inputs with some delays. Figure 3 to figure 6 are represents the outputs of different interconnect lines for in-phase and out-phase switching.

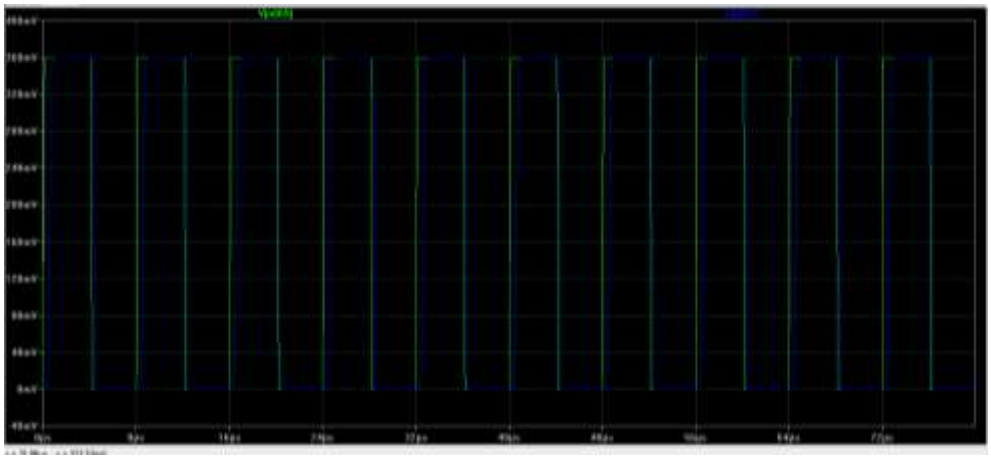

Fig. 5. Output of victim line for out-phase switching

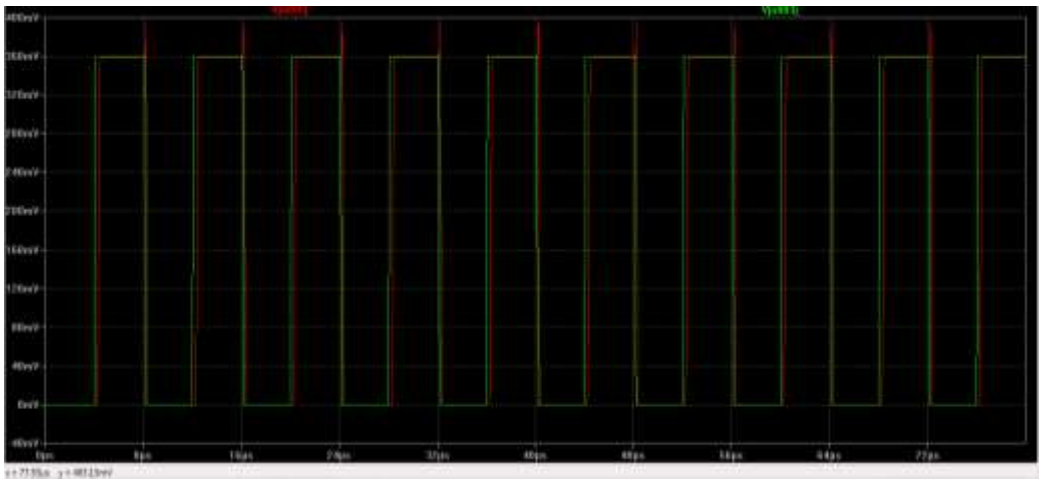

Fig. 6. Output of aggressor line for out-phase switching

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The transition delays for the aggressor interconnect line are given in Table 1. The transition delay for the victim interconnect line is given in table 3. The proposed transition delays for the aggressor interconnect line and victim line as 2.31 and 4.25%, average errors are 2.02 and 3.274%, respectively. Table 2 and Table 4 provide the transition delay and computational error. The proposed method has an average error of 2.3% and maximum error of .6%. In the same way, $\tau p2$ predicted by the proposed method results in average and maximum errors of 1.87 and 2.3%, respectively. All the estimated transition delays are given in Tables 1, 2, 3 and 4.

Table 1. Propagation delay and error involved for aggressor in in-phase switching

W_{n1}(nm)	W_{n2}(nm)	Circuit Parameters					SPICE t_{p1}(ms)	Analytical t_{p1}(ms)	% Error
		R_1(W)	R_2(W)	C_1(pf)	C_2(pf)	C_c(pf)			
97.5	97.5	208.93	208.93	0.30	0.30	0.11	0.1746	0.1734	0.69
97.5	97.5	208.93	208.93	0.20	0.30	0.09	0.1618	0.1606	0.747
97.5	160	208.93	208.93	0.50	0.20	0.11	0.1390	0.1325	4.9
160	97.5	208.93	208.93	0.50	0.20	0.11	1.1556	0.1592	2.31
97.5	292.5	208.93	208.93	0.30	0.30	0.20	0.1211	0.1229	1.48

Table 2. Propagation delay and error involved for aggressor in out-phase switching

W_{n1}(nm)	W_{n2}(nm)	Circuit Parameters					SPICE t_{p1}(ms)	Analytical t_{p1}(ms)	% Error
		R_1(W)	R_2(W)	C_1(pf)	C_2(pf)	C_c(pf)			
97.5	243.7	208.93	208.93	0.3	0.3	0.11	0.2014	0.2056	2.08
97.5	243.7	208.93	208.93	0.3	0.6	0.11	0.1991	0.1951	2.05
97.5	243.7	208.93	208.93	0.6	0.3	0.11	0.2786	0.2731	2.01
97.5	400	208.93	208.93	0.6	0.9	0.11	0.2747	0.2795	1.7
160	243.7	208.93	208.93	0.6	0.6	0.11	0.1880	0.1845	1.8
160	400	208.93	208.93	0.6	0.12	0.21	0.2014	0.2087	3.6
160	400	208.93	208.93	1.2	0.60	0.32	0.3190	0.3100	2.9

Table 3. Propagation delay and error involved for victim in in-phase switching

W_{n1}(nm)	W_{n2}(nm)	Circuit Parameters					SPICE t_{p1}(ms)	Analytical t_{p1}(ms)	% Error
		R_1(W)	R_2(W)	C_1(pf)	C_2(pf)	C_c(pf)			
97.5	97.5	208.93	208.93	0.30	0.30	0.11	0.1735	0.1756	1.21
97.5	97.5	208.93	208.93	0.20	0.30	0.09	0.1607	0.1678	4.41
97.5	160	208.93	208.93	0.50	0.20	0.11	0.1397	0.1452	3.93
160	97.5	208.93	208.93	0.50	0.20	0.11	0.1560	0.1598	2.37
97.5	292.5	208.93	208.93	0.30	0.30	0.20	0.1199	0.1250	4.25

Table 4. Propagation delay and error involved for victim in out-phase switching

W_{n1}(nm)	W_{n2}(nm)	Circuit Parameters					SPICE t_{p1}(ms)	Analytical t_{p1}(ms)	% Error
		R_1(W)	R_2(W)	C_1(pf)	C_2(pf)	C_c(pf)			
97.5	243.7	208.93	208.93	0.3	0.3	0.11	0.1630	0.1666	2.2
97.5	243.7	208.93	208.93	0.3	0.6	0.11	0.2131	0.2181	2.3
97.5	243.7	208.93	208.93	0.6	0.3	0.11	0.1627	0.1654	1.65
97.5	400	208.93	208.93	0.6	0.9	0.11	0.1822	0.1856	1.8
160	243.7	208.93	208.93	0.6	0.6	0.11	0.2131	0.2181	2.3
160	400	208.93	208.93	0.6	0.12	0.21	0.2329	0.2359	1.28
160	400	208.93	208.93	1.2	0.60	0.32	0.1921	0.1951	1.56

4 CONCLUSIONS

In this paper, dynamic crosstalk is analysed for coupled on-chip VLSI interconnects in different conditions. The proposed work has taken the MOS transistor analytical expressions. Based on analytical expressions, calculated the transition delays and different timings of the interconnect aggressor line and interconnect victim line drivers for in-phase transition and out-of-phase change. All the calculated results are compared with simulations in SPICE and proved the proposed analytical model is giving the best results. The average error has been noted in the transmission delay using SPICE is 2.02 and 3.274% for the interconnect aggressor line and interconnect victim line buffers for in phase switching, respectively and average errors in the same are 2.3 and 1.87% for out phase switching event.

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